interrupt circuitry cooperatively designed with the instruction pipeline circuitry to synchronously trigger an interrupt in accordance with interrupt criteria on execution of an instruction of a process, wherein the architectural definition of the instruction does not call for an interrupt, the interrupt criteria being based at least in part on the table entry associated with the address of the instruction, the interrupt circuitry being designed to invoke a handler for the interrupt, the handler being responsive to a content of the table entry to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on the contents of a table entry associated with the address range in which the instruction lies.

#1 end

Kindly add the following new claim:

~~81~~ 77. (new August 27, 2002) A microprocessor chip, comprising:

instruction pipeline circuitry; and

table lookup circuitry designed to retrieve an entry from a table, each entry of the table being associated with a corresponding address range of an address space translated by address translation circuitry of the microprocessor chip, each entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range, the table lookup circuitry operable as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program for execution on the microprocessor chip, the table being stored in storage that is architecturally invisible to programs in the native architecture of at least some instructions executed by the microprocessor chip;

#2

interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger a synchronous interrupt on execution of an instruction of a process, wherein the architectural definition of the instruction of the process does not call for an interrupt, a trigger for the interrupt being synchronously based at least in part on the table entry corresponding to the address of the instruction of the process, the interrupt circuitry being designed to invoke a handler for the interrupt, the handler being responsive to a content of the table entry to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction of the process, based at

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